U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

B/O Form PTO-1390 **Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under *35 USC 371***		*Attorney's Docket Number* GRAS3005
		U.S. Application Number (if known) 09/926791
International Application Number PCT/EP00/05625	*International Filing Date* 19 June 2000	*Priority Date Claimed* 23 June 1999
Title of Invention SEMICONDUCTOR MEMORY CHIP MODULE		
Applicant(s) for DO/EO/US Thomas GRASSL	Assignee	

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items under *35 USC 371*:

1. ☒ This is a **FIRST** submission of items concerning a filing under *35 USC 371*.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under *35 USC 371*.

3. ☒ This express request to begin national examination procedures *(35 USC 371(f))* at any time rather than delay examination until the expiration of the applicable time limit set in *35 USC 371(b)* and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed *35 USC 371(c)(2)*.
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. ☒ A translation of the International Application into English *(35 USC 371(c)(2))*.

7. ☒ Amendments to the claims of the International Application under PCT Article 19 *(35 USC 371(c)(3))*
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 *(35 USC 371(c)(3))*.

9. ☒ An oath or declaration of the inventor(s) *(35 USC 371(c)(4))*. (☐ Executed ☒ Unexecuted)

10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 *(35 USC 371(c)(5))*.

Items 11 to 16 below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under *37 CFR 1.97* and *1.98*.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with *37 CFR 3.28* and *3.31* is included.

13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information: 1 sheet formal drawing

531 Rec'd PCT 20 DEC 2001

Application Number (if known)	International Application Number	Attorney's Docket Number
09/926791	PCT/EP00/05625	GRAS3005/JEK

	Calculations	PTO USE ONLY
17. The following fees are submitted: Basic National Fee *(37 CFR 1.492(a)(1)-(5))*: ☒ Search report has been prepared by the EPO or JPO . . . . . $890.00 ☐ International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* . . . . . $710.00 ☐ No International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* but International Search Fee paid to USPTO *(37 CFR 1.445(a)(2))* . . . . . $740.00 ☐ Neither International Preliminary Examination Fee *(37 CFR 1.482)* nor International Search Fee *(37 CFR 1.445(a)(2))* paid to USPTO . . . . . $1040.00 ☐ International Preliminary Examination Fee paid to USPTO *(37 CFR 1.482)* and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date *(37 CFR 1.492(e))*.		

CLAIMS	NUMBER FILED		NUMBER EXTRA	RATE		
Total Claims	9	-20 =		× $18.00		
Independent Claims	1	-3 =		× $84.00		
Multiple Dependent Claims (if applicable)				+ $280.00		
TOTAL OF ABOVE CALCULATIONS					$ 890.00	
Reduction by ½ for filing by small entity, if applicable. Small Entity Status is asserted pursuant to 37 CFR 1.27 for this application.						
SUBTOTAL					$ 890.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date *(37 CFR 1.492(f))*.						
TOTAL NATIONAL FEE					$ 890.00	
Fee for recording the enclosed assignment *(37 CFR 1.21(h))*. The assignment must be accompanied by an appropriate cover sheet *(37 CFR 3.28, 3.31)*. **$40.00** per property.						
TOTAL FEES ENCLOSED					$ 890.00	
Amount to be:					Refunded:	
					Charged:	

a. ☒ A check in the amount of **$890.00** to cover the fees is enclosed.

b. ☐ Please charge my **Deposit Account Number 02-0200** in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account Number 02-0200**. A duplicate copy of this sheet is enclosed.

Note: Where an appropriate time limit under *37 CFR 1.494* or *1.495* has not been met, a petition to revive *(37 CFR 1.137(a) or (b))* must be filed and granted to restore the application to pending status.

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DATE: 20 December 2001

Respectfully submitted,

E. Ernest Kenney
Attorney for Applicant
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

International Patent Application
No. PCT/EP00/05625

PCT/DO/EO/US

International Filing Date: 19 June 2000

Attorney Docket: GRAS3005/JEK

Applicant: Thomas GRASSL

For: SEMICONDUCTOR MEMORY CHIP MODULE

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper accompanies documents submitted to establish the U.S. national stage of the above-identified international patent application.

The international patent application was amended under PCT Article 34 and the claims as-amended are annexed to the International Preliminary Examination Report (IPER).

Before calculation of the filing fee and before examination, kindly amend the claims as annexed to the IPER as follows:

IN THE CLAIMS:

Please amend the claims as annexed to the IPER as shown on the appended APPENDIX OF CLAIMS, which includes amended and non-amended claims. Also appended hereto an APPENDIX OF MARKED UP CLAIMS showing the changes which have been made.

REMARKS

All rights are reserved to the original claimed subject matter. The claims have been amended to reduce the filing fees and to restate the inventive subject matter in clear terms. None of the amendments are intended to narrow any element of the claims as they stood prior to amendment. Examination of the application as amended is respectfully requested.

Respectfully submitted,
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Date: December 20, 2001

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APPENDIX OF MARKED UP VERSION OF CLAIMS

1(Amended). A semiconductor memory chip module [having] comprising a first memory chip (4) of a first type, a second memory chip (6) of a second type, and an electric connection (14, 16) between the first and second memory chips (4, 6), [characterized in that] wherein the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

2(Amended). A chip module according to claim 1, [characterized in that] wherein memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.

3(Amended). A chip module according to claim 1 [or 2, characterized in that], wherein the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.

4(Amended). A chip module according to [any of claims 1 to 3, characterized in that] claim 1, wherein at least one further chip (8, 16) is provided in a further level.

5(Amended). A chip module according to claim 4, [characterized in that] wherein the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).

6(Amended). A chip module according to [any of claims 1 to 5, characterized in that] claim 1, wherein an energy buffer is formed in at least one of the levels.

7(Amended). A chip module according to claim 6, [characterized in that] wherein the energy buffer is formed as an integrated buffer capacitor (20).

8(Amended). A chip module according to [any of claims 1 to 7] <u>claim 1</u>, formed for a smart card.

9(Amended). A smart card having a semiconductor memory chip module according to [any of claims 1 to 8] <u>claim 1</u>.

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APPENDIX OF CLAIMS

1(Amended). A semiconductor memory chip module comprising a first memory chip (4) of a first type, a second memory chip (6) of a second type, and an electric connection (14, 16) between the first and second memory chips (4, 6), wherein the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

2(Amended). A chip module according to claim 1, wherein memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.

3(Amended). A chip module according to claim 1, wherein the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.

4(Amended). A chip module according to claim 1, wherein at least one further chip (8, 16) is provided in a further level.

5(Amended). A chip module according to claim 4, wherein the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).

6(Amended). A chip module according to claim 1, wherein an energy buffer is formed in at least one of the levels.

7(Amended). A chip module according to claim 6, wherein the energy buffer is formed as an integrated buffer capacitor (20).

8(Amended). A chip module according to claim 1, formed for a smart card.

9(Amended). A smart card having a semiconductor memory chip module according to claim 1.

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Semiconductor memory chip module

This invention relates to a semiconductor memory chip module having a plurality of memory chips of different types, in particular a plurality of memory chips executed in different production technologies. In particular, the invention relates to a semiconductor memory chip module suitable for smart cards and to a smart card equipped with such a chip module.

Currently available semiconductor memories can be assigned to different types in accordance with their production technology, their operating parameters, their capacitance, etc. Semiconductor memories can for example be divided into volatile and nonvolatile memories.

In smart cards and smart card terminals it is expedient to use nonvolatile memories whose content can also be erased and overwritten. Typically used semiconductor memories for such purposes are EEPROMs.

Such EEPROMs, i.e. erasable, electrically programmable read-only memories, necessitate some circuit complexity for erasing and rewriting data and require relatively long access time in comparison to volatile memories, for example a DRAM or SRAM. If such a semiconductor memory is used during execution of software programs, only slow execution is possible for the program. In addition, an EEPROM permits only a limited number of erase and write operations, typically in the range of 10,000 to 100,000.

If the presence of a nonvolatile memory, for example an EEPROM, is required but a rapid-access memory is nevertheless desired for program execution, one idea is to provide in addition to the EEPROM for example a SRAM as a volatile memory which is then used for program execution. If the results are to be stored for some time after execution of a program, the required data can be reloaded to the EEPROM.

The different types of semiconductor memories, that is, in the present case nonvolatile memories (EEPROMs) and rapid volatile memories (SRAMs), are based on different production technologies. If two such different types of semiconductor memories are used side by side, considerable effort is required for operationally interconnecting the two memories. Relatively long conduction paths are necessary between the two memories. This takes up a relatively large portion of the available chip area.

DE 196 26 337 A1 describes the simultaneous use of chips with volatile and nonvolatile memories for storing data. EP 0 328 062 A2 at the same time starts out from use in a smart card, so that EP 0 328 062 A2 has the features of the preamble of the independent claims. However, neither document indicates anything about the geometric structure or arrangement of the chips.

US 5,840,417 describes in general the vertical arrangement and contacting of electronic chips, whereas US 5,229,647 describes the vertical arrangement and contacting of memory chips of the same type. Neither document deals with the problems resulting from the use of different types of memory chips.

The invention is based on the problem of providing a semiconductor memory chip module which permits the advantages of two types of memory chips without the stated disadvantages, that is, high production effort and long conduction paths.

This problem is solved by the features of claim 1. According to the invention, a semiconductor memory chip module with different types of memory chips is formed in that the memory chips are disposed one above the other in different levels and connected by vertical interconnections.

In an especially preferred embodiment, there is a fixed allocation of memory cells of the first memory chip to memory cells of the second memory chip, the mutually allocated memory cells being directly interconnected by the vertical connections.

In an especially preferred embodiment, the first type of memory chip is a nonvolatile memory, in particular EEPROM, and the second type a volatile memory, for example a SRAM.

The invention allows production of a semiconductor memory chip module having different types of memory chips, in particular memory chips fabricated by different production technologies. The chips can according to the invention be produced separately, with the aid of the production processes typical of them. The finished chips require relatively little chip area in each case. The finished chips are then stacked, the connections between the chips being vertical connections, i.e. requiring very little additional chip area. The chip stack is then formed as a self-contained unit, in particular packaged into one module, so that it can be mounted in a smart card.

In the simplest embodiment of the invention, two chip levels can be provided. Since each semiconductor memory includes not only the actual memory cells but also a drive circuit, referred to as a decoder here, said decoders can be formed together with the particular semiconductor chip. In an especially advantageous embodiment of the invention, however, it is provided that a further chip with decoder circuits for all memory chips of the chip module is provided in a further level. The chip occupying area is thus not increased - in the horizontal direction - by the decoder circuits in the further chip. The chip with the decoder circuits is also connected by vertical chip interconnections to the memory chip of the first or second type, depending on which chip is located directly under the chip with the decoder circuits.

A special feature in using memory chips in connection with smart cards and smart card terminals is the protection from so-called power analysis attacks. In such attacks an attempt is made with fraudulent intent to analyze current and voltage states on a circuit with the aid of special sensors in order to be able to infer protected data. If voltage and current levels which always assume one, or one of several, defined levels independently of internal circuit states are ensured on all connections, such an attack is impossible.

A constantly recharged capacitor, a so-called buffer capacitor, can be used to smooth the supply voltage for the chip to such an extent that no level changes are outwardly recognizable which could permit circuit states to be inferred.

In a preferred embodiment of the invention it is provided that an energy buffer, in particular in the form of an integrated capacitor, is formed in at least one of the levels of the chip module. Said buffer capacitor can occupy a total chip level, but in a preferred multilayer design it can also be limited only to a partial chip area so that the rest of this level is available for memory cells, decoder circuits or logic circuits. Said buffer capacitor can be used, at the end of processing of a program performed with the aid of the volatile memory, to store the results of the program and further data in the nonvolatile memory. In case of a program abortion caused by external disturbing influences for example, the data necessary for restarting the program can be stored permanently in the nonvolatile memory with the aid of the buffer capacitor.

In the following, some examples of the invention will be explained in more detail with reference to the drawing, in which:

Figure 1 shows a schematic vertical sectional view of a semiconductor memory chip module according to a first embodiment of the invention; and

Figure 2 shows a view similar to Figure 1 of a second embodiment of the invention.

Figure 1 shows semiconductor memory chip module 2 according to a first embodiment of the invention. Chip module 2 contains three stacked chips, namely bottom chip 4, formed here as an EEPROM, i.e. a nonvolatile memory chip, middle chip 6, formed here as an SRAM, i.e. a volatile memory chip, and top chip 8 comprising two types of decoder circuits 10 and 12.

Memory chip 4 contains a predetermined number of memory cells C4. Aligned therewith in the vertical direction, memory chip 6 contains a corresponding number of volatile memory cells C6.

Memory cells C4 and C6 in memory chips 4 and 6 are vertically aligned, as indicated by vertical lines in Figure 1. Between mutually vertically allocated memory cells C4 and C6 there is a direct electric connection through so-called vertical chip interconnections, to be explained in more detail below for the example shown in Figure 2.

Decoder circuits 10 and 12 contained in the top level in top chip 8 permit different addressing capabilities for memory chips 4 and 6. In the present embodiment, decoder circuits 10 (only one being shown in Figure 1) serve to drive memory cells C4 in bottom memory chip 4 while decoder circuits 12 serve to drive memory cells C6 in middle memory chip 6. In a modified embodiment, however, decoder circuits 10 and 12 can also be used for both memory chips 4 and 6 in each case.

Figure 2 shows a second embodiment of semiconductor memory chip module 2' which is structured on the basis of the chip module shown in Figure 1.

As in the first embodiment, bottom chip 4 is formed as an EEPROM, in the next level above is chip 6 formed as an SRAM. Mutually vertically aligned memory cells C4 and C6 are directly connected electrically by vertical chip interconnections 16.

Similar vertical chip interconnections connect memory chip 6 with chip 8, which contains decoder circuits (not shown in detail) and additionally buffer capacitor 20. Buffer capacitor 20 is likewise connected by direct vertical chip interconnections 22a with memory chip 6 located below and by chip interconnections 22b with further chip

16 located above, and is furthermore connected by a connection indicated at 24 with the decoder circuits contained in chip 8. Through connections not shown also connect buffer capacitor 20 with bottom memory chip 4.

Semiconductor memory chip module 2' of the embodiment shown in Figure 2 contains not only buffer capacitor 20, which acts as an energy buffer, but also chip 16 in an uppermost level, said chip containing for example logic circuits whose function is available for all other chips 4, 6 and 8.

In the embodiment according to Figure 2, buffer capacitor 20 is produced from a plurality of alternating electroconductive and dielectric layers. A feeder (not shown) is used to hold buffer capacitor 20 constantly at a supply voltage level. Its capacitance is such that it allows data to be written from the SRAM of memory chip 6 to corresponding memory cells of the EEPROM of memory chip 4 in the case of service abortion of chip module 2' for example.

The invention and the embodiments of a chip module shown in Figures 1 and 2 are suitable in particular for incorporation in a smart card or smart card terminal, albeit the invention is not limited thereto. As a further modification of the invention, the order of the memory chips can be altered. In Figure 1 various chips 4, 6 and 8 can have their order changed for example. The same holds for the arrangement according to Figure 2. Buffer capacitor 20 can also extend over a total chip level. The decoder circuits, shown at 10 and 12 in top chip 8 in Figure 1, can also be distributed over different chip levels.

The examples of semiconductor memory chip modules shown in Figures 1 and 2 contain chips 4, 6, 8 and 16 fabricated in separate production processes. The separately fabricated chips are stacked and vertically interconnected by bonding. Bonding refers in this case to connecting the individual chips or wafers containing chips. For this purpose the chips or wafers can be thinned, i.e. their thickness reduced after production. The actual electric interconnection of the individual chips or wafers is effected by vertical chip interconnections, as described above. The vertical chip interconnections are produced by a metalization process corresponding to the metalization process during production of the individual chips or wafers. This permits a high connection density, which e.g. allows individual memory cells to be interconnected electrically in different levels, i.e. on different chips, as described above. This moreover causes an increase in

above. This moreover causes an increase in security since the internal vertical chip interconnections are not accessible from outside and thus cannot be tapped for analysis purposes.

The thus obtained total arrangement is encased and then available for mounting in a smart card for example. Encasing including the outwardly guided interconnecting leads will not be explained in detail here because it is conventional.

When mounted in a smart card the semiconductor memory chip module according to Figure 1 or Figure 2 works in such a way that the permanently stored data are located in bottom chip 4, that is, in the nonvolatile memory EEPROM. Upon execution of programs, required data are reloaded to the middle chip, that is, the volatile memory (SRAM). Middle chip 6 then acts like a cache memory. Result data and data to be protected in case of service abortion for example are then reloaded from middle memory chip 6 to bottom memory chip 4, using the energy stored in the buffer capacitor.

Claims

1. A semiconductor memory chip module having a first memory chip (4) of a first type, a second memory chip (6) of a second type, and an electric connection (14, 16) between the first and second memory chips (4, 6), characterized in that the memory chips (4, 6) are disposed one above the other in different levels and connected by vertical chip interconnections (14, 16).

2. A chip module according to claim 1, characterized in that memory cells (C4) of the first memory chip (4) are firmly allocated to certain memory cells (C6) of the second memory chip (6), and the mutually allocated memory cells (C4, C6) are directly interconnected electrically.

3. A chip module according to claim 1 or 2, characterized in that the first type corresponds to a nonvolatile memory, for example EEPROM, and the second type to a volatile memory, for example SRAM.

4. A chip module according to any of claims 1 to 3, characterized in that at least one further chip (8, 16) is provided in a further level.

5. A chip module according to claim 4, characterized in that the further chip contains decoder circuits (10, 12) for the memory chips (4, 6).

6. A chip module according to any of claims 1 to 5, characterized in that an energy buffer is formed in at least one of the levels.

7. A chip module according to claim 6, characterized in that the energy buffer is formed as an integrated buffer capacitor (20).

8. A chip module according to any of claims 1 to 7, formed for a smart card.

9. A smart card having a semiconductor memory chip module according to any of claims 1 to 8.

FIG.1

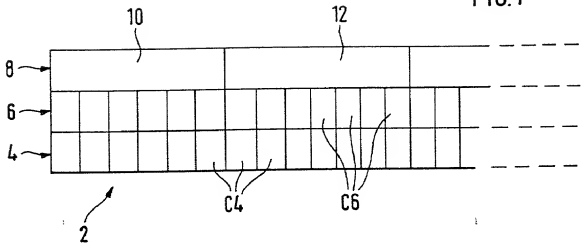
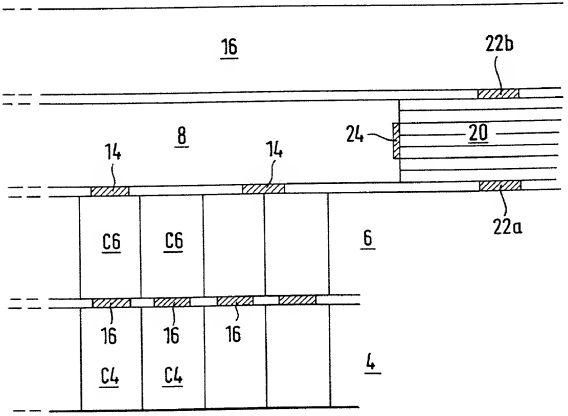


FIG.2



ATTORNEY DOCKET NO: **GRAS3005/JEK**

DECLARATION FOR PATENT APPLICATION AND APPOINTMENT OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name; I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention (Design, if applicable) entitled:

SEMICONDUCTOR MEMORY CHIP MODULE

the specification of which (check one):

☐ is attached hereto, or ☒ was filed on: **19 June 2000** as U.S. Application Number or PCT International Application Number: **PCT/EP00/05625** and (if applicable) was amended on:

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56*. I hereby claim foreign priority benefits under *Title 35, United States Code §119* of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	**Country**	**Day/Month/Year Filed**	**Yes**	**No**
199 28 733.3	Germany	23 June 1999	X	

☐ Additional Priority Application(s) Listed on Following Page(s)

I HEREBY CLAIM THE BENEFIT UNDER TITLE 35 U.S. CODE §119(E) OF ANY U.S. PROVISIONAL APPLICATIONS LISTED BELOW.	
Application Number	**Day/Month/Year Filed**

☐ Additional Provisional Application(s) Listed on Following Page(s)

I hereby claim the benefit under *Title 35, United States Code, §120* of any United States application(s) or PCT international application(s) designating The United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of *Title 35, United States Code, §112*, I acknowledge the duty to disclose information which is material to patentability as defined in *Title 37, Code of Federal Regulations, §1.56* which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Number	Filing Date	Status - Patented, Pending or Abandoned

☐ Additional US/PCT Priority Application(s) listed on Following Page(s)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under *section 1001 of title 18 of the United States Code* and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: I (We) hereby appoint as my (our) attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: J. Ernest Kenney, Reg. No. 19,179; Eugene Mar, Reg. No. 25,893; Richard E. Fichter, Reg. No. 26,382; Thomas J. Moore, Reg. No. 28,974; Joseph DeBenedictis, Reg. No. 28,502; Benjamin E. Urcia, Reg. No. 33,805; and

I(we) authorize my(our) attorneys to accept and follow instructions from **Klunker, Schmitt-Nilson, Hirsch** regarding any matter related to the preparation, examination, grant and maintenance of this application, any continuation, continuation-in-part or divisional based thereon, and any patent resulting therefrom, until I(we) or my(our) assigns withdraw this authorization in writing.

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DATE 08.03.2002	SIGNATURE

☐ *See following page(s) for additional joint inventors.*